Express Mail Label No. EK 069304165 US 03-22-00 A

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. 1109
Total Pages in this Submission

JC658 U.S. PTO 03/21/00

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

JC639 U.S. PTO 09/532144 03/21/00

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

LAYER SEQUENCE BUIL ON A SUBSTRATE IN THIN-FILM TECHNOLOGY

and invented by:

Martin SCHALLNER, Soeren STEINERT

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having 12 pages and including the following:

   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. 1109
Total Pages in this Submission

Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*

   a. ☒ Formal Number of Sheets 2

   b. ☐ Informal Number of Sheets

4. ☒ Oath or Declaration

   a. ☐ Newly executed *(original or copy)* ☒ Unexecuted

   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*

   c. ☒ With Power of Attorney ☐ Without Power of Attorney

   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*

   a. ☐ Paper Copy

   b. ☐ Computer Readable Copy *(identical to computer copy)*

   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing

    ☐ First Class ☒ Express Mail *(Specify Label No.):* EK 069304165 US

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. 1109
Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

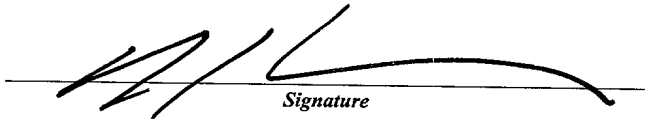
CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	11	- 20 =	0	x	$18.00	$0.00
Indep. Claims	2	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
OTHER FEE *(specify purpose)* _____						
					TOTAL FILING FEE	$690.00

☒ A check in the amount of **$690.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **19-4675** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).



Signature

Dated: **MARCH 21, 2000**

cc:

BE IT KNOWN that **We**, Martin SCHALLNER and Soeren STEINERT, citizens of Germany, whose post office addresses and residencies are respectively, Wimpfener Strasse 6, 71642 Ludwigsburg, Germany; and Schwenninger Strasse 33, 71522 Backnang Germany; have invented a certain new and useful

LAYER SEQUENCE BUILT ON A SUBSTRATE IN THIN-FILM TECHNOLOGY

Of which the following is a complete specification thereof:

BACKGROUND OF THE INVENTION

The present invention relates to a layer sequence built on a substrate in thin-film technology and, more particularly, to a layer sequence comprising an electrically conductive sputtered layer, which is reinforced by a similar electrical conductive reinforcing layer, which is applied to the electrically conductive sputtered layer by a method other than sputtering.

Laser adjustment of resistors has been used for many years to adjust operation and to compensate for manufacturing tolerances in the field of thin-film and thick-film technology. The resistors on substrates or boards are adjusted to their set value, before the substrates or boards are equipped with components, or to a computed resistance value according to the component characteristic values (e.g. capacitance). A slight amount of residue is produced by the adjustment because of the type of material being worked. This residue can be removed, if necessary, after the adjustment by cleaning.

Furthermore for a few years metallic conductive layers (e.g. Gold layers) have been removed or eroded from capacitors, in order to change their capacitance and thus to be able, for example, to adjust the resonance frequencies of oscillator circuits (Lasertrim Capacitors, Johnson Technology, Camarillo, CA). This adjustment is also an operational adjustment. Of course extraneous contaminant material is produced during this adjustment procedure near the adjusted locations, but this contaminant material is of little significance for these

components in housings, since they are used in connection with adjustable capacitors in the frequency range of up to a few 100 MHz.

However laser adjustment of (metallic conductive) thin-film structures, for example of resonators formed from structured gold on ceramic material (see tuning of ring resonators as described in the still unpublished German Patent Application 198 21 382) is new. Here also an operational adjustment is performed.

During laser erosion of 3 to 5 μm thick gold layers, as often employed in thin-film technology, gold-containing deposits with particle sizes of up to a few tens of micrometers arise. These deposits are very problematical, since open semiconductors (e.g. transistors with 0.25 μm gate structures) are often used in thin-film technology, which are comparatively sensitive to extraneous contaminant material. A cleaning to remove the residue formed by the adjustment is only possible in certain special cases, since the operational adjustment primarily occurs with the components completely assembled on the board or chip. During an adjustment the extraneous deposited particles are only partially removed by vacuuming techniques.

Summary of the Invention

It is an object of the present invention to provide a layer sequence on a substrate of the above-described type, which avoids the above-described disadvantage during an adjustment performed by using a laser to remove material.

These objects, and others, which will be made more apparent hereinafter, are attained in a layer sequence comprising an electrically conductive sputtered layer, which is reinforced by a similar electrically conductive reinforcing layer, which is applied to the electrically conductive sputtered layer by another method.

According to the invention regions of the electrically conductive sputtered layer to be adjusted, i.e. by the laser adjustment method, are not reinforced by the reinforcing layers as much as the remaining portions of the electrically conductive sputtered layer.

Extraneous contaminant material produced by the laser erosion or removal method during an adjustment can be minimized with the layer structure according to the invention, which is shown by the following disclosure.

In a conventional layer sequence in thin-layer technology according to figure 1 an adherent sputtered layer 2 having a thickness of a few tens of nanometers is provided first on a substrate 1. Then a sputtered resistor layer 3 with a thickness of the same order of magnitude as the first sputtered adherent layer 2 is applied over it. Then similarly a gold sputtered layer 4 having a thickness in a range between about 200 nm and 400 nm is applied over the sputtered resistor layer 3. Finally an

additional gold reinforcing layer 5, which was produced by galvanic deposition, chemical reinforcement or physically (for example by rolling on or spraying), having a thickness of about 2 to 10 micrometers was provided on the gold sputtered layer 4.

The above-described contamination problem is largely avoided because the reinforcement of the conductive sputtered layer is completely or partially eliminated in the regions in which the laser adjustment is to be performed. Because of that feature the material erosion during the adjustment is considerably reduced. Thus, for example, when the reinforcing layer is completely removed from a location or region to be adjusted, a sputtered layer of only about 300 nm is removed during the adjustment, instead of a 5 μm thick reinforcing gold layer. Because of that the amount of eroded or removed material is reduced by about 94 %. Furthermore the conductive sputtered layer is essentially more fine-grained than the reinforcing layer, so that particles arising during laser adjustment are correspondingly smaller and vaporize.

However because of the reduced layer thickness the surface resistance of the remaining layers increases and thus current losses increase. However at high frequencies this increase is small, since the current scarcely penetrates into the conductor because of skin effect and only flows in a thin layer in the conductor surface. The current losses are proportional to the existing current density. The increase of losses because of the thinner conductive layer sequence can be minimized because the adjusted regions, if circuit engineering techniques permit, are provided in regions, in which no or only a small amount of current flows, for

example at the end of an open conductor. Furthermore the adjusted regions are generally small in comparison to the entire conductor structure. Consequently the local increase of the surface resistance has scarcely any effect on the losses of the entire conductor structure.

In circuits, in which some increase in losses is tolerable, the entire board or substrate can also be provided with a thin conductive layer, whereby processing effort and thus expenses are reduced. Generally assembly of components or connections by means of bonding wires is expensive.

Additional advantageous embodiments are set forth in the dependent claims appended hereinbelow, whose features, as far as it is significant, may be combined with each other.

Brief Description of the Drawing

The objects, features and advantages of the invention will now be illustrated in more detail with the aid of the following description of the preferred embodiments, with reference to the accompanying figures in which:

Figure 1 is a schematic cross-sectional view through a layer sequence of the prior art;

Figure 2 is plan view of a chip capacitor;

Figure 3 is a side view of a the chip capacitor;

Figure 4 is a side view of a ceramic capacitor in SMD technology;

Figure 5 is a plan view of an end of an open-circuit strip line;

Figure 6 is a plan view of a ring resonator; and

Figure 7 is a connecting line.

Parts in different figures that are substantially the same are given the same reference numbers.

Description of the Preferred Embodiments

The figures show several examples including optimized layer sequences according to the invention.

Figures 2 and 3 show a chip capacitor, which is metallized on its upper and lower side surfaces. If only a part of the surface on the upper side in a region 6 to be adjusted is coated with a thin metal layer, it can be adjusted. The portion 7 of the upper surface or top surface with the conventional layer sequence of Fig. 1 and bonding wire 8 act as a connector for the upper capacitor side. A solder or adhesive connection 9 is made to the substrate 1 on the lower side of the capacitor.

The entire upper covering metal layer 10 can be made thin in ceramic capacitors in SMD technology (see Lasertrim Capacitors, Johnson Technology, Camarillo, CA). A multi-layer ceramic capacitor in SMD technology is shown in Fig. 4 with its contacting surfaces 11 and 12 for adhesives or solder.

For adjusting of the conductor length of an open-circuit strip line 13 the metallization at the open conductor end 14 is made thin, as shown in Fig.5.

The resonance frequency of the ring resonator 15 shown in Fig. 6 can be changed by targeted incisions or cuts made by laser. Also the metallization in the regions 16, 17 to be adjusted is thin (see German Patent Application 198 21 382).

If adjustments of a conducting line 18, which for example is used as a connecting conductor for different components, are required, as shown in Figure 7, the region 19 to be adjusted is metallized comparatively thin.

The disclosure in German Patent Application 199 13 466.9 of March 25, 1999 is incorporated here by reference. This German Patent Application describes the invention described hereinabove and claimed in the claims appended hereinbelow and provides the basis for a claim of priority for the instant invention under 35 U.S.C. 119.

While the invention has been illustrated and described as embodied in a new layer sequence in thin-layer technology, it is not intended to be limited to the details shown, since various modifications and changes may be made without departing in any way from the spirit of the present invention.

Without further analysis, the foregoing will so fully reveal the gist of the present invention that others can, by applying current knowledge, readily adapt it for various applications without omitting features that, from the standpoint of prior art, fairly constitute essential characteristics of the generic or specific aspects of this invention.

What is claimed is new and is set forth in the following appended claims.

We claim:

1. A layer sequence built on a substrate in thin-layer technology, said layer sequence comprising an electrically conductive sputtered layer (4) and an electrically conductive reinforcing layer (5) for reinforcing or strengthening the sputtered layer, said reinforcing layer (5) being applied by a method other than sputtering, wherein said electrically conductive reinforcing layer (5) is made a less effective reinforcing means for the sputtered layer in regions (6,10,14, 16, 17, 19) of said electrically conductive sputtered layer (4) to be adjusted than in other regions outside of said regions to be adjusted.

2. The layer sequence as defined in claim 1, wherein said electrically conductive reinforcing layer (5) is thinner in said regions (6,10,14, 16, 17, 19) of said electrically conductive sputtered layer (4) to be adjusted than in said other regions.

3. The layer sequence as defined in claim 1, wherein said electrically conductive sputtered layer (4) is made of gold.

4. The layer sequence as defined in claim 1, wherein said electrically conductive reinforcing layer (5) is made of gold.

5. The layer sequence as defined in claim 1, wherein said regions (14, 16, 17) of said electrically conductive sputtered layer (4) to be adjusted are located in portions of the layer sequence carrying less current than other portions.

6. The layer sequence as defined in claim 5, wherein at least one of said regions (14, 16, 17) of said electrically conductive sputtered layer (4) to be adjusted is located at an end of an open conducting line (13).

7. The layer sequence as defined in claim 2, wherein said other regions outside of said regions (14, 16, 17) of said electrically conductive sputtered layer (4) to be adjusted include contacting surfaces (11,12).

8. The layer sequence as defined in claim 1, wherein said regions (14, 16, 17) of said electrically conductive sputtered layer (4) to be adjusted are located on a side of said sputtered layer (4) opposite from said substrate (1).

9. A layer sequence built on a substrate in thin-layer technology, said layer sequence comprising an electrically conductive sputtered layer (4) and an electrically conductive reinforcing layer (5) for reinforcing or strengthening the sputtered layer, said reinforcing layer (5) being applied by a method other than sputtering, wherein said electrically conductive reinforcing layer (5) has a smaller thickness in regions (6,10,14, 16, 17, 19) of said electrically conductive sputtered layer (4) to be adjusted than in other regions outside of said regions to be adjusted.

10. The layer sequence as defined in claim 9, wherein said electrically conductive reinforcing layer (5) is eliminated from said regions (6,10,14, 16, 17, 19) of said electrically conductive sputtered layer (4) to be adjusted.

11. The layer sequence as defined in claim 9, wherein said sputtered layer (4) and said reinforcing layer (5) are both made of gold.

ABSTRACT OF THE DISCLOSURE

The layer sequence built on a substrate in thin-layer technology includes an electrically conductive sputtered layer (4) and an electrically conductive reinforcing layer (5) for reinforcing or strengthening the sputtered layer, which is applied by a method other than sputtering. In order to remove conducting material with the aid of a laser for the purposes of adjustment while producing as little contaminating material as possible, the electrically conductive reinforcing layer (5) has a reduced thickness or is completely eliminated in regions (6,10,14, 16, 17, 19) of the electrically conductive sputtered layer (4) to be adjusted than in other regions outside of the regions to be adjusted.

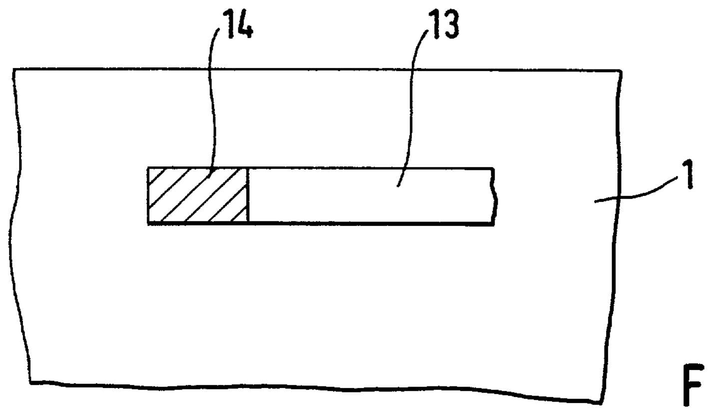


Fig.5

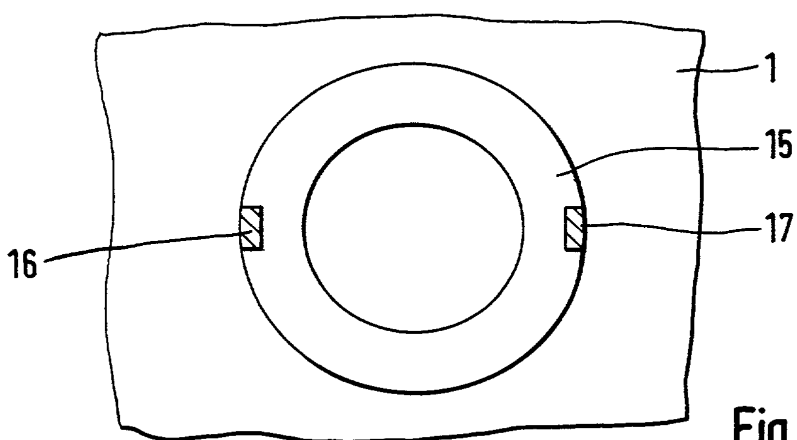


Fig.6

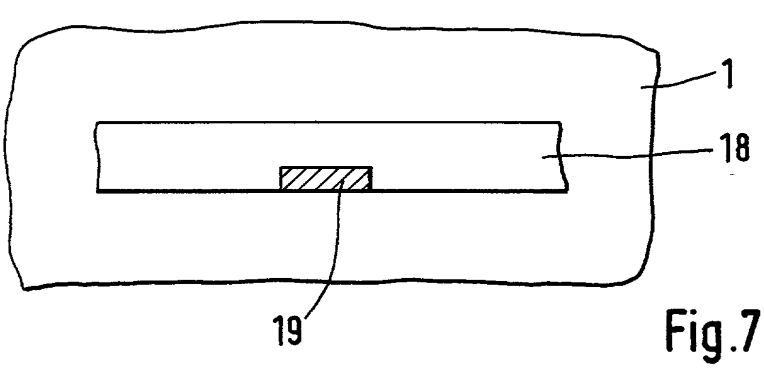


Fig.7

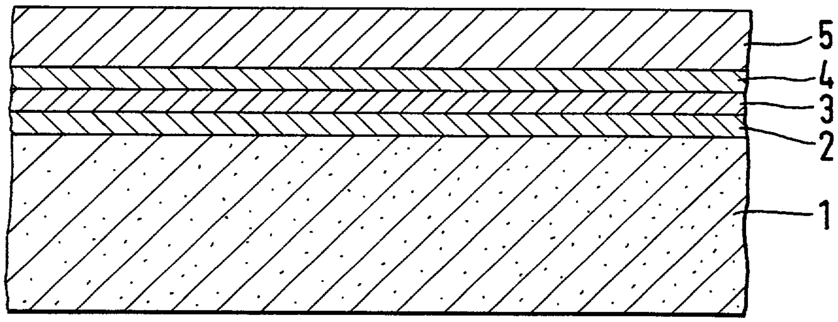


Fig.1

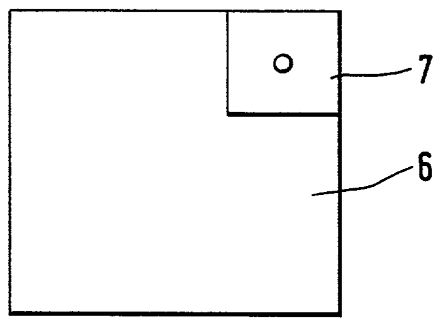


Fig.2

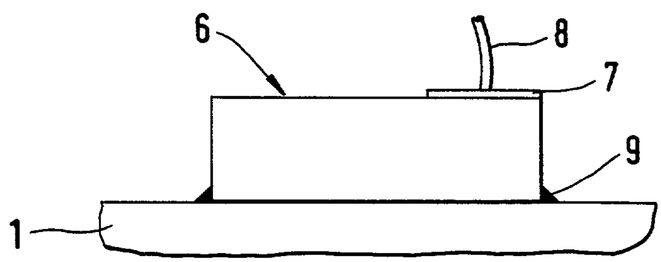


Fig.3

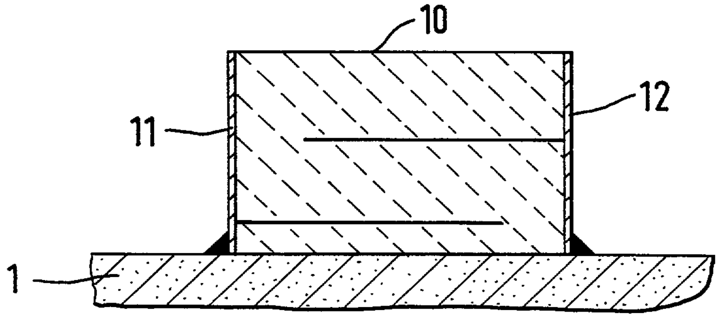


Fig.4

PTO/SB/103 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney for Patent Application
Erklärung für Patentanmeldungen mit Vollmacht

GermanLanguageDeclaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

Martin SCHALLNER
Soeren STEINERT

dass mein Wohnsitz, meine Postanschrift und meine Staatsangehörigkeit den im nachstehenden nach meinem Namen aufgeführten Angaben entsprechen, dass ich nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent für die Erfindung mit folgendem Titel beantragt wird:

AUF EINEM SUBSTRAT AUFGEBAUTE SCHICHTENFOLGE IN DÜNNSCHICHTTECHNOLOGIE

deren Beschreibung hier beigefügt ist, es sei denn (in diesem Falle Zutreffendes bitte ankreuzen), diese Erfindung

☐ wurde angemeldet am_____
unter der US-Anmeldenummer oder unter der Internationalen Anmeldenummer im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesens (PCT)
_____und am
_____abgeändert (falls zutreffend).

Ich bestätige hiermit, dass ich den Inhalt der oben angegebenen Patentanmeldung, einschliesslich der Ansprüche, die eventuell durch einen oben erwähnten Zusatzantrag abgeändert wurde, durchgesehen und verstanden habe.

Ich erkenne meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Titel 37, § 1.56 von Belang sind.

As a below named inventor, I hereby declare that:

Martin SCHALLNER
Soeren STEINERT

My residence, post office address and citizenship are as stated next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LAYER SEQUENCE BUILT ON A SUBSTRATE IN THIN-FILM TECHNOLOGY

the specification of which is attached hereto unless the following box is checked:

☐ was filed on_____
as United States Application Number or PCT International Application Number
_____and was amended on
_____(if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Code of Federal Regulations, Regulations, § 1.56.

PTO/SB/103 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

GermanLanguageDeclaration

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Title 35, US-Code, § 119 (a)-(d), bzw. § 365(b) aller unten aufgeführten Auslandsanmeldungen für Patente oder Erfinderurkunden, oder § 365(a)aller PCT internationalen Anmeldungen, welche wenigstens ein Land ausser den Vereinigten Staaten von Amerika benennen, und habe nachstehend durch ankreuzen sämtliche Auslands-anmeldungen für Patente bzw. Erfinderurkunden oder PCT internationale Anmeldungen angegeben, deren Anmeldetag dem der Anmeldung, für welche Priorität beansprucht wird, vorangeht.

I hereby claim foreign priority under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Applications
(Frühere ausländische Anmeldungen)

Priority Not Claimed
Priorität nicht beansprucht

(Number) (Nummer)	(Country) (Land)	(Day/Month/Year Filed) (Tag/Monat/Jahr der Anmeldung)	
199 13 466.9	GERMANY	MARCH 25, 1999	☐
			☐

Ich beanspruche hiermit Prioritätsvorteile unter Title 35, US-Code, § 119(e) aller US-Hilfsanmeldungen wie unten aufgezählt.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s)listed below.

(Application No.) (Akzenzeichen)	(Filing Date) (Anmeldetag)

Ich beanspruche hiermit die mir unter Title 35, US-Code, § 120 zustehenden Vorteile aller unten aufgeführten US-Patentanmeldungen bzw. § 365(c) aller PCT internationalen Anmeldungen, welche die Vereinigten Staaten von Amerika benennen, und erkenne, insofern der Gegenstand eines jeden früheren Anspruchs dieser Patentanmeldung nicht in einer US-Patentanmeldung, bzw. PCT internationalen Anmeldung in in einer gemäss dem ersten Absatz von Title 35, US-Code, § 112 vorgeschriebenen Art und Weise offenbart wurde, meine Pflicht zur Offenbarung jeglicher Informationen an, die zur Prüfung der Patentfähigkeit in Einklang mit Title 37, Code of Federal Regulations, § 1.56 von Belang sind und die im Zeitraum zwischen dem Anmeldetag der früheren Patentanmeldung und dem nationalen oder im Rahmen des Vertrags über die Zusammenarbeit auf dem Gebiet des Patentwesen (PCT) gültigen internationalen Anmeldetags bekannt geworden sind.

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application No.) (Akzenzeichen)	(Filing Date) (Anmeldentag)	(Status) (patented, pending, abandoned) (Status) (pateniert, schwebend, aufgegeben)
(Application No.) (Akzenzeichen)	(Filing Date) (Anmeldentag)	(Status) (patented, pending, abandoned) (Status) (pateniert, schwebend, aufgegeben)

Ich erkläre hiermit, dass alle in der vorliegenden Erklärung von mir gemachten Angaben nach bestem Wissen und Gewissen der Wahrheit entsprechen, und ferner dass ich diese eidesstattliche Erklärung in Kenntnis dessen ablege, dass wissentlich und vorsätzlich falsche Angaben oder dergleichen gemäss § 1001, Title 18 des US-Code strafbar sind und mit Geldstrafe und/oder Gefängnis bestraft werden können und dass derartige wissentlich und vorsätzlich falsche Angaben die Rechtswirksamkeit der vorliegenden Patentanmeldung oder eines aufgrund deren erteilten Patentes gefährden können..

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief arebelieved to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/103 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

GermanLanguageDeclaration

VERTRETUNGSVOLMACHT: Als benannter Erfinder beauftrage ich hiermit den (die) nachstehend aufgeführten Patentanwalt (älte) und/oder Vertreter mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Angelegenheiten vor dem US-Patent- und Markenamt: *(Name(n) und Registrationsnummer(n) auflisten)*

Michael J. Striker, Registration No. 27233
Ilya Zborovsky, Registration No. 28563
William G. Valance, Registration No.: 28275

Postanschrift
STRIKER, STRIKER & STENBY
103 East Neck Road
Huntington, NY 11743

Telefonische Auskünfte (Name und Telefonnummer)

Michael J. Striker
(631) 549 4700

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

Michael J. Striker, Registration No. 27233
Ilya Zborovsky, Registration No. 28563
William G. Valance, Registration No.: 28275

Send Correspondence to:
STRIKER, STRIKER & STENBY
103 East Neck Road
Huntington, NY 11743

Direct Telephone Calls to:

Michael J. Striker
(631) 549 4700

Vor- und Zuname des einzigen oder ersten Erfinders Martin SCHALLNER	Full name of sole or first inventor Martin SCHALLNER
Unterschrift des Erfinders Datum	Inventor's signature Date
Wohnsitz Wimpfener Strasse 6, 71642 Ludwigsburg, Germany	Residence Wimpfener Strasse 6, 71642 Ludwigsburg, Germany
Staatangehörtigkeit GERMANY	Citizenship GERMANY
Postanschrift Wimpfener Strasse 6, 71642 Ludwigsburg, Germany	Post Office Address Wimpfener Strasse 6, 71642 Ludwigsburg, Germany
Vor- und Zuname des zweitens Erfinders (falls zutreffend) Soeren STEINERT	Full name of second joint inventor, if any Soeren STEINERT
Unterschrift des Erfinders Datum	Second inventor's signature Date
Wohnsitz Schwenninger Strasse 33, 71522 Backnang, Germany	Residence Schwenninger Strasse 33, 71522 Backnang, Germany
Staatangehörtigkeit GERMANY	Citizenship GERMANY
Postanschrift Schwenninger Strasse 33, 71522 Backnang, Germany	Post Office Address Schwenninger Strasse 33, 71522 Backnang, Germany